Vertical-Cavity Surface Emitting Laser (VCSEL)

Introduction

1.1 Background

Diode laser applications

Today, diode lasers find wide-spread use in areas ranging from medical therapeutic, material treatment, entertainment and optical data storage to fiber optic telecommunication systems. Most people know the bright red laser beam from a hand held laser pointer. On the other side, in the large majority of other consumer electronic products such as compact disc (CD) or digital versatile disc (DVD) players and in laser printers the diode lasers are hidden from the human eye.

The most important applications of diode lasers are in telecommunication and in optical data storage. Telecommunication lasers constitute more than two thirds of the total diode laser market [1], and their importance is steadily increasing. The driving force is the internet, which has created an insatiable demand for high bit-rate transfer of large data volumes. The involved data pipelines are built with fiber optic systems today.

High modulation speed lasers are used for the signal transmission through the optical fibers, while pump lasers reprocess the signal every $\sim 100\,km$ in erbium-doped fiber amplifiers (EDFAs) [2]. Modern installations use wavelength-division-multiplexed (WDM) systems, where many (for example 32 [3]) lasers with closely spaced wavelengths are used to send different signals in parallel through a single optical fiber.

While telecommunication systems offer high data rates, the installation of such systems is expensive. Local area networks (LANs), which locally interconnect a company's computers, require more cost-effective solutions. In contrast to telecommunications, the laser is an important cost factor in these systems. Typically, the distances involved in LANs are limited to a few hundred meters, where signal attenuation and dispersion in the fiber are less critical than in telecommunications. Vertical-cavity surface-emitting lasers (VCSELs) with a wavelength of $850\,nm$ are a cost effective solution, and therefore emerge as the preferred transmitter unit in this relatively new field. Even though LANs make up only a few percent of the total diode laser market today, the annual growth rate of more than 130 % in 1999 [1] is higher than in the other fields. Therefore, VCSELs are likely to become an important breed of diode lasers in the next few years.

Edge emitters and vertical-cavity surface-emitting lasers

The first lasing action in semiconductors was achieved with an edge emitting laser in 1962 [4]. Since then, many refinements have been applied and the performance of edge emitting lasers has tremendously been improved. An overview over different designs is given in [5].

In edge emitters, the light propagates in the plane of the active layer, which is parallel to the wafer surface. The optical cavity is formed between two cleaved semiconductor facets. In contrast to this in-plane cavity, Iga [6] proposed a revolutionary approach for making a diode

laser in 1977: In a vertical-cavity surface-emitting laser (VCSEL) the cavity is formed in the direction perpendicular to the active layer. The laser mirrors in this device are no longer cleaved semiconductor/air interfaces, but specially designed multi-layer mirrors in the plane of the wafer surface. Due to the technological difficulty of fabricating the required highly reflective in-plane mirrors, the first room temperature operation of a VCSEL was demonstrated only 12 years later in 1989 [7]. Today, VCSELs have matured enough to find their way from research laboratories to the first commercial applications.

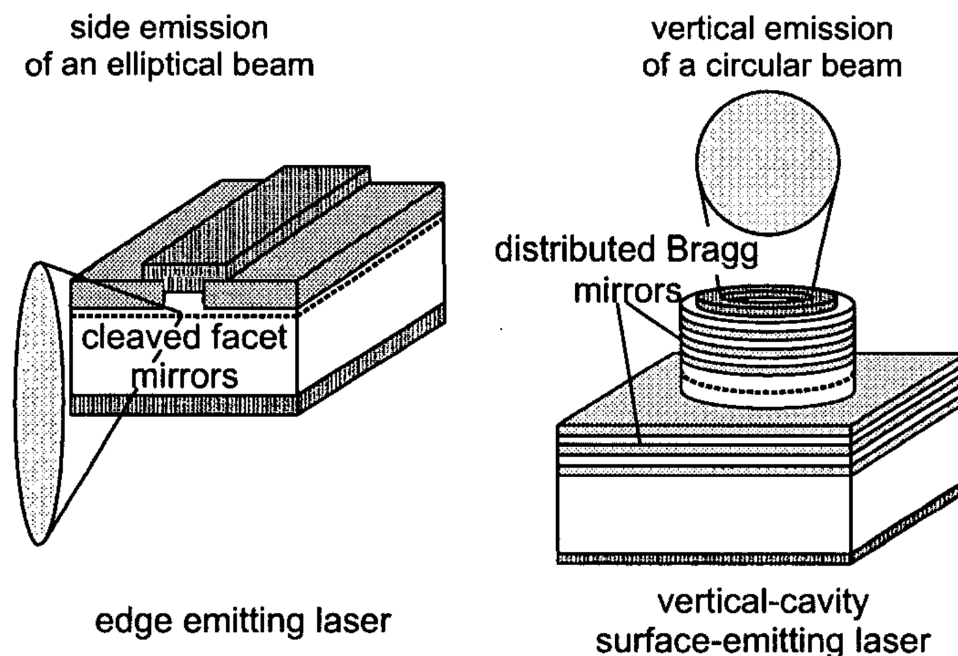


Figure 1.1: Schematic drawings of an edge emitting laser (left) and a vertical-cavity surface-emitting laser (right).

Figure 1.1 compares the basic geometry of a conventional edge emitting laser with that of a VCSEL. The VCSEL geometry offers several advantages:

- The top emitting design allows to complete all processing steps and testing on the wafer level. In contrast to that, edge emitting

lasers must be cleaved into individual devices before they can be operated and tested.

- VCSELs can be fabricated in the form of two dimensional arrays, which may be used for parallel data processing or image displays.

- Due to their short cavity length, VCSELs inherently emit in a single longitudinal mode. With current or temperature tuning, the emission wavelength can be continuously adjusted over a relatively wide spectral range. Single longitudinal mode operation in edge emitters requires difficult and expensive processing steps.

- VCSELs emit a circularly symmetric, low divergent beam, which can efficiently be coupled into an optical fiber without the need of expensive optics.

- The small active volume of a VCSEL leads to a very low threshold current and to a low power consumption.

- VCSELs can be modulated at relatively high speed ($\sim 10\,Ghz$).

These properties make VCSELs well suited for many applications, including gas sensing [8], pumping of atomic clocks [9], free-space and fiber based optical data interconnects [10]. The ease of production and testing of VCSELs gives them a large potential cost advantage over edge emitting lasers. The low divergence, circular emission beam simplifies the design of external optics, cutting down system costs even further.

However, there are also a few reasons why VCSELs have not pushed edge emitting lasers from the market. The wavelength range, in which VCSEL technology is mature enough today limits their use to only a few applications: There are no commercially available VCSELs emitting at $650\,nm$ or shorter wavelength, which would be required for

DVD lasers or laser pointers. VCSELs emitting at the telecommunication wavelengths of 1.3 and 1.55 μm are not yet available either, in spite of some prototype demonstrations. Other problems of VCSELs are multi-transverse mode operation, polarization switches, and limited output power. Therefore, even though VCSELs offer many advantages, their industrial use is limited today primarily to the field of local area networks.

Chapter 3: Threshold conditions and mirror design for a VCSEL structure

3.1 Introduction

A vertical cavity surface emitting laser (VCSEL) is a semiconductor laser diode emitting light in the direction perpendicular to the wafer surface. In contrast to edge emitting lasers diodes (LDs), the cavity and the laser mirrors are arranged in the vertical *z* direction, as shown in figure 3.1. Electrons and holes are injected into the structure through the mirrors or by using intracavity contacts. The injected carriers recombine radiatively in the *p-n* junction located inside the cavity formed by the two mirrors. The gain region is formed by quantum wells (QWs) sandwiched between the *p*-layer and the *n*-layer.

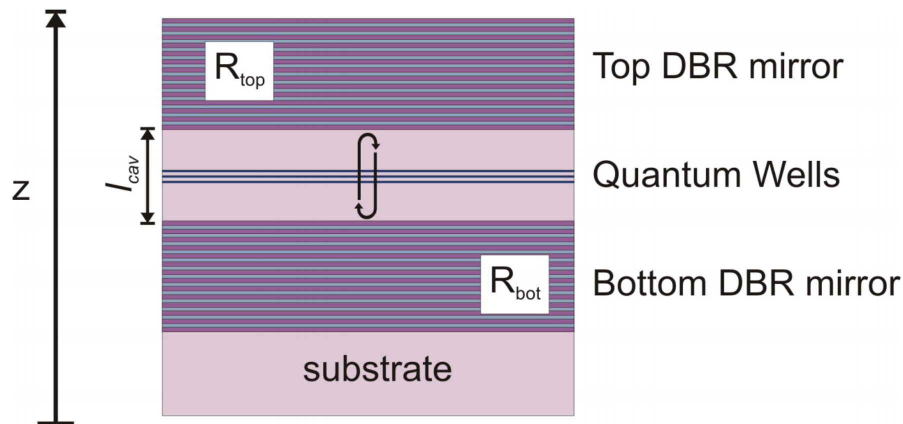


Figure 3.1: Schematic section of a planar VCSEL structure. The physical cavity length is $l_{cav} = \lambda/n$, where n is the refractive index of the cavity material and λ the lasing wavelength. The reflectivity of the DBRs usually exceeds 99%. Both the current injection and the light emission occur along the vertical direction (*z*-axis).

The principal difference between a VCSEL and an edge emitting LD is represented by the shorter cavity length of the VCSEL. Its length is of the order of a single wavelength, while for edge emitting LDs it is a few hundreds microns. Because of this, only a few single longitudinal modes are supported by a VCSEL cavity.

Moreover, the emission wavelength is not determined anymore by the maximum gain of the active material but rather by the geometry of the cavity. Thus, VCSELs can lase only if the QW emission wavelength approximately coincides with the cavity mode. Another consequence of the short cavity length is that VCSELs are not affected by mode-hopping induced by thermal heating.

Lasing in a VCSEL critically depends (as it will be explained in the following paragraphs) on the reflectivity of both the top and bottom mirrors. Values above 99% can be reached by using distributed Bragg reflectors (DBRs), consisting of several stacks of $\lambda/4$ bilayers made of a low and high refractive index materials, respectively. The DBRs can be epitaxially grown or can be dielectric and thus, deposited afterwards.

3.2 The threshold condition

In this section, we try to predict a threshold current density for our VCSEL structures based on the threshold gain.

The lasing condition in a laser is reached when the amplitude of the optical field is maintained after a round trip in the cavity [1]. This condition is reached when the optical gain in the cavity is sufficient to compensate all the losses the field experiences in the cavity during a round trip. These losses can be divided in internal losses (due to absorption, scattering and diffraction) and external losses (due to the light output through the mirrors).

The threshold condition, without taking into account scattering and diffraction losses, can be written as

$$\langle g_{th} \rangle = \Gamma_{xy}\Gamma_z g_{th} = \alpha_i + \frac{1}{l_{cav}} \ln\left(\frac{1}{R}\right), \qquad \textbf{(3.1)}$$

where $\langle g_{th} \rangle$ is the threshold modal gain, Γ_{xy} and Γ_z are the confinement factors in the transverse directions and propagation direction respectively, g_{th} is the threshold material gain, l_{cav} is the cavity length, α_i the absorption coefficient of the cavity and R is the average mirror reflectivity.

$$R = \sqrt{R_{top} R_{bot}} \qquad \textbf{(3.2)}$$

with R_{top} and R_{bot} the top mirror reflectivity and the bottom one, respectively. These last two values take also into account the absorption losses in the mirrors.

The confinement factors (Γ_{xy} and Γ_z) accounts for the volume actually occupied by photons in the cavity, that is usually larger than the active region volume [1]. Considering a good confinement in the axial directions (Γ_{xy} = 1) Γ_z can be approximated as:

$$\Gamma_z = \frac{l_{act}}{l_{cav}} \quad \textbf{(3.3)}$$

While for an edge emitting LD this value is equal to 1, in a VCSEL Γ_z assumes a smaller value. Anyway, it has to be pointed out, that when l_{act} is smaller than λ, Γ_z is subject to an enhancement dependent on the position of the active region into the cavity. The standing wave enhancement factor Γ_{enh} is defined by the equation:

$$\Gamma_{enh} = \frac{1}{l_{act}} \int_{QWs} \frac{2|E(z)|^2}{|E_0|^2} dz \,, \quad \textbf{(3.4)}$$

where $|E(z)|^2$ is the square of the electric field in the cavity, and $|E_0|^2$ is the maximum value. As it can be easily depicted, in an edge emitting structure Γ_{enh} is equal to one, since the average value of the light intensity $\overline{|E(z)|^2}$ along the propagation direction is equal to half of the maximum value $|E_0|^2$.

In a VCSEL structure, where the length of the active region is much shorter than one wavelength, the QWs have to be positioned correctly, as Γ_{enh} may vary from 0 to 2. If the wells are positioned at a field node (E(z) = 0), there will be no interaction in between the optical field and the active material. In this case, Γ_{enh} will be equal to 0. On the contrary, if the QWs are placed at a cavity light field antinode, *i.e.* at a maximum of the field propagating in the cavity, Γ_{enh} will be close to 2 (figure 3.2).

For a VCSEL, the confinement factor in the propagation direction becomes then:

$$\Gamma'_z = \Gamma_z \Gamma_{enh} \quad \textbf{(3.5)}$$

For the structures considered in this work (3 QWs of 3 nm each, a 5λ/2 cavity length), we find Γ'_z = 0.035, with Γ_z =0.021 and Γ_{enh} = 1.62.

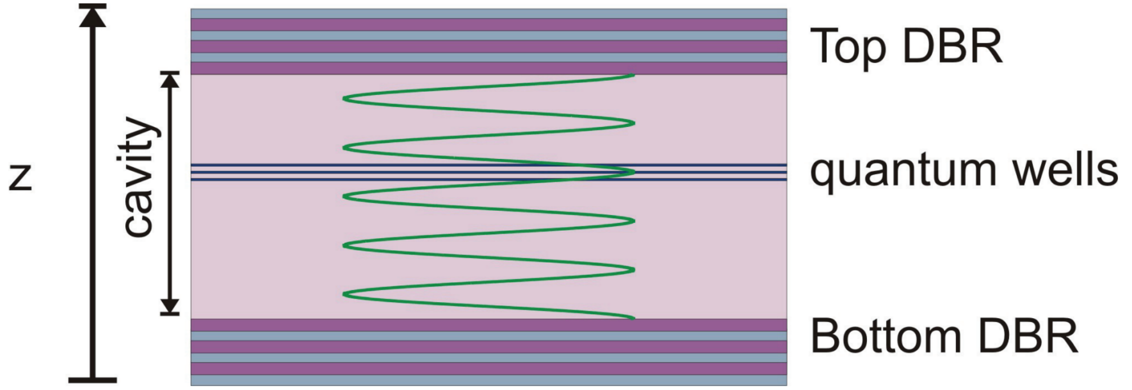


Figure 3.2: Longitudinal field distribution inside a VCSEL (5λ/2 cavity) structure along the z-axis. The QWs have to be placed close to a field antinode in order to have a maximum interaction.

The gain versus current relation can be calculated with theoretical models [1]. Here, the following experimental relation will be used:

$$\langle g_{th} \rangle = \Gamma_z^{'} g_{th} = N_{QW} g_0 \ln\left(\frac{J_{th}}{N_{QW} J_{tr}}\right) \quad \textbf{(3.6)}$$

where g_0 is the gain parameter per QW, J_{th} the total current density at the threshold and J_{tr} is the current density at transparency per QW. Since gain and losses in a device are strongly dependent on the quality of the crystal structure, the estimation of these values for GaN-based VCSEL structures is far to be trivial.

For the edge emitters, the gain parameter was estimated to be $g_0 = 25$ cm^{-1}, the current transparency $J_{tr} = 0.65$ kA/ cm^2, and the internal losses $\alpha_i = 22$ cm^{-1}. These values however, have to be taken with extreme prudence since they depend on a correct evaluation of the mirror reflectivities. A good estimation of the reflectivity of the edge emitter facets is difficult to obtain so the reported data are affected by some uncertainty. Anyway, by using them, a clear picture of the impact of mirror losses on the threshold current and on the gain can be obtained. In Table 3.1 all the values of the above mentioned parameters are listed for a 5λ/2 cavity having either one, three or five QWs, 3 nm thick, separated by 12 nm thick GaN barriers.

Parameter	Value		
N_{QW}	1	3	5
l_{act}	3 nm	9 nm	15 nm
l_{cav}	422.5 nm		
Γ_z	0.007	0.021	0.036
Γ_{enh}	1.99	1.62	1.13
α_i	22 cm^{-1}		
$N_{QW}{\cdot}g_0$	25 cm^{-1}	75 cm^{-1}	125 cm^{-1}
$N_{QW}{\cdot}J_{tr}$	0.65 kA/cm^2	2 kA/cm^2	3.3 kA/cm^2

Table 3.1: List of the parameters used in the estimation of the threshold current density as a function of the average mirrors reflectivity R.

Combining Eqn. (3.1) and Eqn. (3.6), a prediction of the threshold current density J_{th} as a function of the average mirror reflectivity R can be done. Results are shown in figure 3.3.

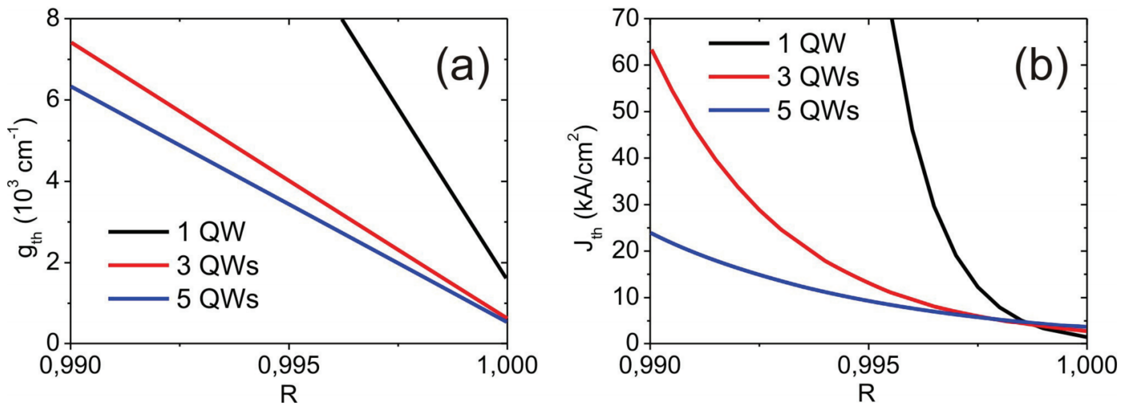


Figure 3.3: (a) Threshold gain and (b) threshold current density as a function of the average mirror reflectivity R for a 5λ/2 cavity having 1, 3 or 5 QWs. The values used for the parameters are reported in Table 3.1.

For very high mirror reflectivities ($R \approx 99.9\%$), a single QW device has the lowest threshold current because it requires the smallest current density to be pumped at the transparency. In devices having more than one QW, the current density at the transparency will be proportional to the number of QWs and so will be the current density at threshold. For lower mirror reflectivities, the necessary current densities will be higher and the higher threshold gain, required to overcome the mirror losses in

a roundtrip in the cavity, will lead to higher threshold current densities in the single QW device compared to the MQW structures.

Assuming a reflectivity of 99.5%, the current densities needed to achieve the lasing condition are 13 kA/cm^2 and 9 kA/cm^2 for the structures with three and five QWs, respectively.

Although the five QW structure could seem to be the better solution, it has to be considered that the calculations do not take into account the fact than in GaN based emitting structures the injection is not uniform in all the QWs. The carrier injection will be more efficient into the QWs close to the *p*-type layer, while it will decrease when moving towards the substrate. Moreover, any non pumped QW will represent a source of absorption, increasing, hence, the internal losses. Considering high reflectivity mirrors and taking into account the results shown in Chapter, 2 we decided to develop a structure including only three QWs in the final structure.

Other possible loss mechanisms include scattering at interfaces, and diffraction losses.

3.3 Evaluation of the mirror characteristics

In the previous section we observed that, in order to achieve the lasing condition in a VCSEL structure for reasonable current densities, mirrors reflectivity must be at least equal to 99.5%. Metal reflectors are not suitable since they show high absorption around 400 nm and in any case they do not reach the reflectivities required for this specific purpose. Hence, distributed Bragg reflectors (DBRs) (dielectric or epitaxial) remain the only candidates. Before addressing the issue of the specific materials, it is necessary to give some basic notions about the parameters that determine the DBR characteristics. Based on the concept of constructive interference, DBRs provide a very high reflectivity for a given design wavelength λ_0.

The reflection coefficient of an incident plane wave at a dielectric interface can be obtained from the boundary conditions of the electric and magnetic field at the discontinuity. In the case of normal incidence, the reflection coefficient of a wave traveling from a material having a high index of refraction (n_H) to a material with a low index (n_L) is:

$$r = \frac{n_H - n_L}{n_H + n_L} \quad \textbf{(3.9)}$$

A DBR consists of a periodic multilayer structure alternating high and low refractive index materials. The thickness of every layer is chosen to be:

$$d = \frac{\lambda_0}{4n} \quad \textbf{(3.10)}$$

where λ_0 is the design wavelength and n is the refractive index of the layer.

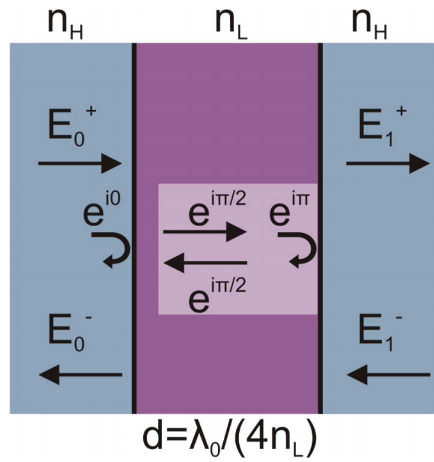


Figure 3.5: Detail of one period of a DBR mirror. The optical thickness of each layer is $\lambda_0/4$. In this way, the phase contribution to the reflected wave is a multiple of 2π.

The phase of the wave reflected at the first interface is 0 (figure 3.5) while the phase of the reflected wave at the second discontinuity will be 2π. Hence, the two contributions will sum constructively in phase at the design wavelength λ_0. The needed reflectivity values are obtained by increasing the number of periods in the structure.

The reflectivity of the DBR, at the design wavelength, is a function of the difference in index of refraction between the two layer types (n_H and n_L) and the number of periods as given by equation (3.11):

$$R = |r_{DBR}|^2 = \left(\frac{1-b}{1+b}\right)^2 \quad \textbf{(3.11)}$$

where r_{DBR} is the reflection coefficient of the DBR and the coefficient b depends from the parity of the number of periods:

$$b_{even} = \frac{n_{out}}{n_{in}} \left(\frac{n_H}{n_L} \right)^{2m}$$

$$b_{odd} = \frac{n_H^2}{n_{in} n_{out}} \left(\frac{n_H}{n_L} \right)^{2m} \quad \textbf{(3.12)}$$

Here, n_{in} and n_{out} are the indices of refraction of the media at the "input" discontinuity and at the "output" discontinuity of the DBR, respectively. As it can be easily depicted from equations (3.11) and (3.12), the higher is the index contrast, the fewer are the periods needed to reach reflectivities exceeding 99%. The spectral width of the high reflectivity region (called stop-band) is also dependent on the index contrast:

$$\Delta\lambda_{stopband} = \frac{2\lambda_0}{\pi n_{eff}} \Delta n \quad \textbf{(3.13)}$$

where n_{eff} and Δn are given by:

$$n_{eff} = 2 \left(\frac{1}{n_H} + \frac{1}{n_L} \right)^{-1}$$

$$\Delta n = n_H - n_L \quad \textbf{(3.14)}$$

Given the difficulties in growing uniform active regions in GaN based heterostructures, a mirror with a wide stop-band would ensure a higher tolerance with respect to emission wavelength variations.

Finally, the penetration of the optical mode into the DBR stack has to be taken into account, as it defines the effective cavity length and, subsequently, the wavelength of the lasing mode. The penetration depth l_{eff} of the DBR is defined as the depth into the mirror, at which the optical field intensity is equal to 1/e of its value at the input of the mirror. For a large number of periods, it can be approximated by:

$$l_{eff} = \frac{\lambda_0}{4\Delta n} \quad \textbf{(3.15)}$$

Figure 3.6 shows how the optical field penetrates into a DBR. The wave coming from the left is reflected at each discontinuity interface and the interference of incident and reflected components gives rise to a standing wave pattern. The penetration depth allows approximating the DBR to a single surface mirror, placed at a distance l_{eff} from the cavity.

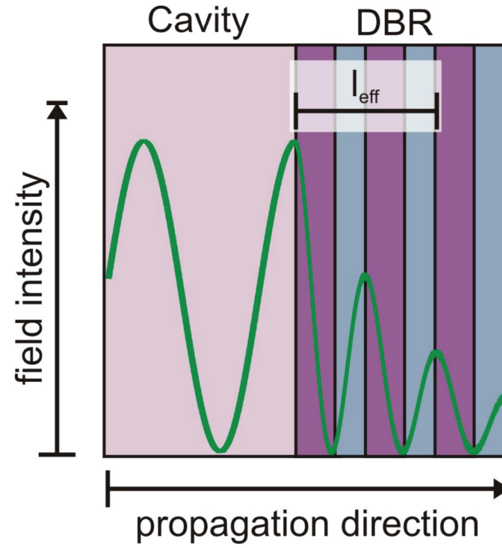


Figure 3.6: Field intensity decay inside the DBR.

Finally, it must be considered that DBRs are also affected by absorption losses. If α_{DBR} is the absorption coefficient of the dielectric mirror, and R_m the reflectivity of an m-pair DBR at the design wavelength λ_0, the reflectivity will be reduced to:

$$R_\alpha = R_m \exp(-2\alpha_{DBR} l_{eff}) \quad \textbf{(3.16)}$$

For an infinite number of periods, given the material system, the maximum achievable reflectivity will be thus:

$$R_{MAX} = R_\alpha (m \to \infty) = 1 \cdot \exp\left(-\frac{\alpha_{DBR}\lambda_0}{2\Delta n}\right) \quad \textbf{(3.17)}$$

For a more complete determination of the DBR spectral characteristics, the transfer matrix formalism can be adopted. To our purpose, the notions provided above are sufficient.

In our cavity design, an epitaxially grown AlInN/GaN bottom DBR and a dielectric SiO_2/Si_3N_4 top DBR are included into the structure. In the following sections, their realization and characteristics are discussed.

Effetti delle perdite per assorbimento

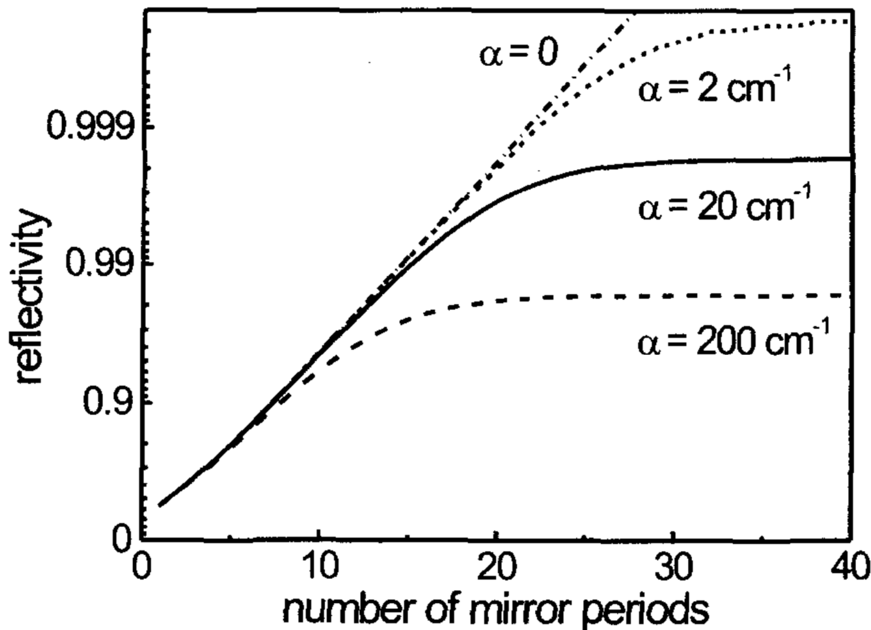


Figure 2.7: Reflectivity of a DBR mirror at the Bragg frequency calculated as a function of the number of mirror periods. While the lossless calculation allows arbitrary high reflectivities to be obtained, the calculations with loss converge to a reflectivity smaller than 1. Note that for zero mirror periods, the curves extrapolate to $R = 0.31$, the interface reflectivity between $GaAs$ and air.

Besides low material loss, a high index step Δn between the mirror layers helps to reduce the mirror loss caused by absorption. In long wavelength VCSELs, which emit at 1.3 or 1.55 μm, all three parameters appearing in the exponent of Equation 2.11 tend to be worse for the mirror material that is used here. Absorption loss is therefore one of the largest problems for long wavelength VCSELs.

Figure 2.7 compares the reflectivity obtained from the lossless calculation 2.5 to that calculated with 2.10. For a large number of periods, the mirror reflectivity saturates to the value given by Equation 2.11. For a targeted reflectivity of 99 %, the necessary number of periods is 15, assuming an absorption coefficient of $\alpha = 14\,cm^{-1}$ and abrupt

mirror interfaces.

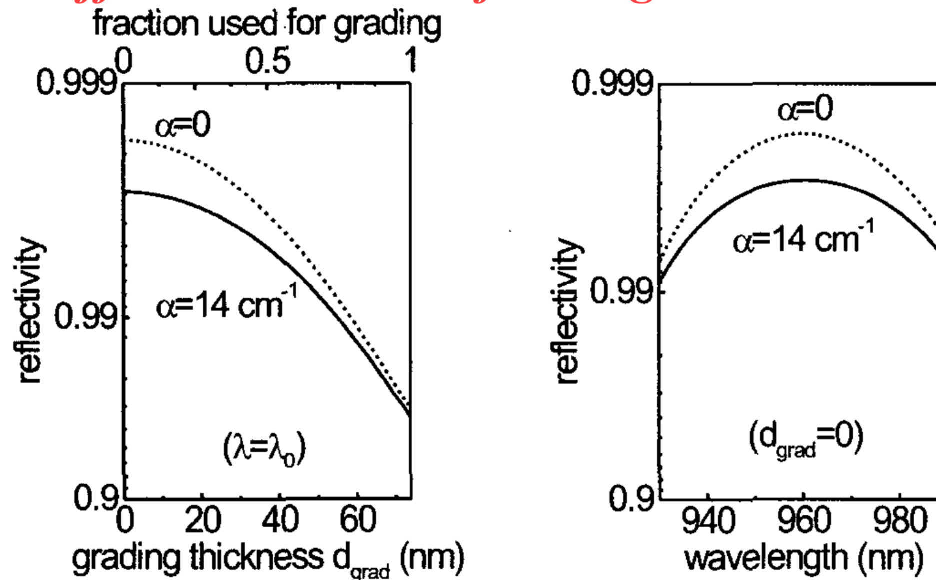


Figure 2.8: a) Effect of a linear grading on the reflectivity, and b) Reflectivity for wavelengths other than $\lambda_0 = 960\,nm$ in a 20-period $GaAs/Al_{0.9}Ga_{0.1}As$ DBR. The curves were calculated both for a lossless mirror (dashed curve) and a mirror with an absorption coefficient of $14\,cm^{-1}$.

Besides absorption, two other effects which can reduce the reflectivity of a Bragg mirror must be considered. First of all, the mirror interfaces in our structures are not abrupt, but the material composition is linearly graded over a distance of $30\,nm$ to reduce the electrical resistance across the interface. (see Section 2.1.3). This also leads to a graded index profile, which lowers the reflectivity of the interface. Figure 2.8 a) shows the reflectivity of a 20 period $Al_{0.9}Ga_{0.1}As/GaAs$ mirror calculated as a function of the grading thickness. The reflectivity reduction for thin gradings is very small: Even if half of a $\lambda_0/4$ layer is graded, the reflectivity of the mirror remains above 99.4 %. The chosen grading thickness of $30\,nm$ in our mirrors is about 40 % of the thickness of a $\lambda_0/4$ layer. Including both absorption and grading in the calculations, the top mirror must contain 17 periods to obtain a reflectivity of 99 %.

The second effect which can reduce the reflectivity in VCSELs is due to a detuned cavity length, as the one shown in Figure 2.6. The wavelength of the laser mode in such a structure is slightly different from the mirror wavelength λ_0. Figure 2.8 b) shows the reflectivity for wavelengths in the vicinity of the mirror design wavelength, again for a 20 period $Al_{0.9}Ga_{0.1}As/GaAs$ DBR. For the case of a VCSEL, we find that the growth errors are sufficiently small, so that in practise the cavity wavelength is always within $5\,nm$ of the mirror wavelength, where the reflectivity reduction is below 0.01 %.

The plots in Figure 2.8 were calculated with a transmission matrix program. Analytical approximations for the two effects reducing the mirror reflectivity can be obtained from coupled mode theory, as explained in [29, 33].

Mirror transmission

Energy conservation in a DBR mirror implies that

$$1 = R + T + A \tag{2.12}$$

where R is the reflectivity, T the mirror transmission and A the power loss of the mirror caused by absorption. The threshold condition of the laser demands only that the reflectivity of the mirrors is high. In this sense, both A and T are loss factors for the laser. For a given A, the lowest threshold would be obtained with $T = 0$. However, in such a closed resonator, no light would be coupled to the outside and thus the efficiency would be zero.

To fabricate a highly efficient top emitting VCSEL, it is important that the transmission through the top mirror is large in comparison to the other losses of the resonator. In Section 2.1.4, the efficiency

to be high, since the light coupled out of the bottom will not be collected.

2.1.3 Electrical carrier injection

Injection of electrical carriers into the active region of the laser involves two parts: The principal task of carrier injection is to confine the carriers to the gain region. Unconfined carriers will recombine in areas where they do not contribute to the laser gain. This will increase the threshold current and reduce the efficiency.

The second issue concerning carrier injection is to keep the electrical device resistance as low as possible. A high electrical resistance will increase the voltage drop over the device and thereby reduce the wallplug efficiency of the VCSEL. It will also produce ohmic heating, which normally degrades the performance of the device. A low ohmic resistance R is further important for high speed modulation, since the resistance will increase the parasitic time constant $\tau = RC$ of the laser (where C is the VCSEL capacitance).

Mirror resistance

Electrical current is applied to a VCSEL either with intracavity contacts [34] or by injection through the DBR mirrors. We chose the latter approach since current crowding near the perimeter of the device is less pronounced and the fabrication technology is simpler. However, with a top contact the current must flow through the DBR mirror and the heterointerfaces in the mirror will increase the electrical resistance of a device. This section describes how the electrical resistance can be kept low, while a high mirror reflectivity is maintained.

The electrical conductivity σ of a DBR mirror is expected to be different in the plane of the mirrors (σ_{xy}) and perpendicular to the het-

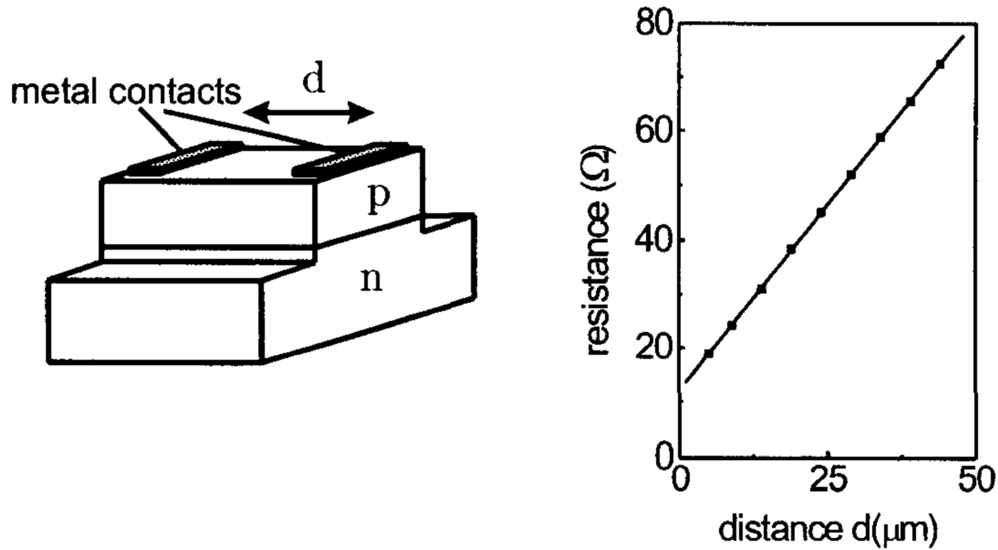


Figure 2.10: The drawing shows a test structure used to measure the in-plane conductivity with the transfer length method, which is described in [35]. The conductivity is inversely related to the sheet resistance, which is given by the slope of the measurement curve shown on the right side.

erointerfaces (σ_z). While the device resistance is determined mainly by σ_z, current spreading in the mirrors, which will be simulated in Section 2.2.1 depends on the relative magnitude of the two conductivities. The in-plane conductivity is simply related to the carrier concentration N and the mobility μ of the carriers by (q is the electrical unit charge):

$$\sigma_{xy} = q\mu N \tag{2.13}$$

For different conductivities in the high and low index layers of the mirror, the in-plane mirror conductivity is given by a simple weighted average. Equation 2.13 means that conductivity can be increased by using a high doping concentration. Since electrons have the higher mobility than holes [36], the conductivity in the n-mirror will be higher than in the p-mirror. In our VCSELs the mesa is etched only through the top p-mirror but not through the n-mirror, which together with the lower conductivity means that the device resistance

will mostly be affected by the p-side of the structure. Therefore, only the p-mirror resistance is considered in the following.

The in-plane conductivity of the p-mirror can be measured on a complete VCSEL structure with the transfer length method [35]. Besides the conductivity, the contact resistance of the semiconductor/metal contact is simultaneously obtained. Figure 2.10 shows a schematic drawing of a test structure and a sample measurement curve. From this curve, a value of $\sigma_{xy} = 46\,(\Omega cm)^{-1}$ is determined in our VCSEL structure. This is about 40 % lower than expected from Equation 2.13 using the design doping level of $2 \cdot 10^{18}\,cm^{-3}$ and the mobilities given in Appendix C.

The vertical mirror conductivity will certainly be lower than the in-plane conductivity, due to the mirror heterointerfaces. For a calculation of the interface resistances, the heterojunction between $GaAs$ and $Al_{0.9}Ga_{0.1}As$ must be considered. Heterojunctions are described, for example, in [37]. $GaAs$ and $Al_{0.9}Ga_{0.1}As$ form a type I heterostructure, which means that wells are formed for both holes and electrons in the low bandgap material. Figure 2.11 a) shows the relative band alignment when the two materials are separated from each other. The position of the indicated Fermi potential Φ_F corresponds to a p-doped material with a doping level of $p = 10^{18}\,cm^{-3}$, which is also shown in the top of the Figure.

When a junction between the two materials is formed, holes will flow from $Al_{0.9}Ga_{0.1}As$ to $GaAs$ and form space charge regions until the Fermi levels are aligned. This is shown in Figure 2.11 b). The $Al_{0.9}Ga_{0.1}As$ becomes depleted near the interface, and on the $GaAs$ side accumulation occurs. The movement of charge gives rise to the band bending near the interface needed to align the Fermi levels under equilibrium conditions. For the illustration in Figure 2.11, the *SimWindows* software [38] was used. The same program will be used in the following to simulate the voltage drop across differently designed interfaces. The program solves the Poisson equation together with the continuity equations for both electrons and holes.

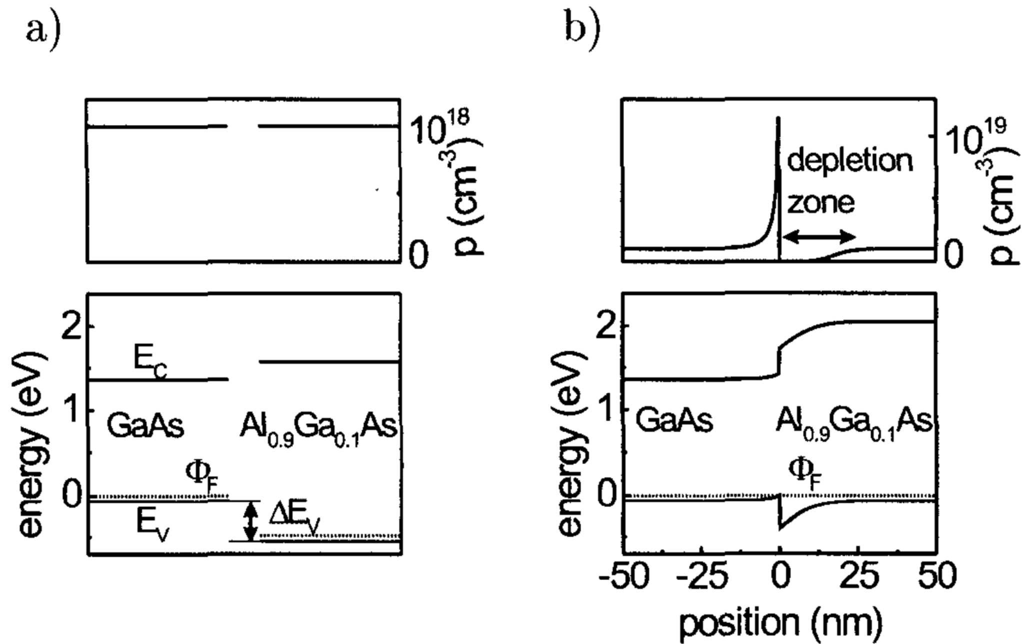


Figure 2.11: Band edges E_C (conduction band) and E_V (valence band) and Fermi potential Φ_F of $GaAs$ and $Al_{0.9}Ga_{0.1}As$ a) before, and b) after contact is made. A doping level of $10^{18}\,cm^{-3}$ is assumed and the hole concentration p is plotted in the top of the Figures.

The material parameters used for the simulations are summarized in Appendix C.

Under bias conditions, the spike in the valence band edge at the junction forms a barrier for the injected carriers. The height E_{bar} of this potential spike, as indicated in Figure 2.12, is nearly equal to the valence band offset $\Delta E_V = 440 meV$ of the two materials. If the applied voltage is lower than this barrier height, the carriers must flow across the junction by either tunneling or thermal emission. With a barrier width of about $20\,nm$ tunneling is very unlikely, and the thermal energy of the carriers is too small for thermal emission over the barrier height of $330\,meV$. Therefore, a very high resistance must be expected. The interface resistance will again be higher for holes than for electrons, because the valence band offset is larger than the conduction band offset. In addition, the larger hole mass

also reduces tunneling and thermionic emission.

A compositional grading at the heterointerface is an efficient way to lower the barrier height. Figure 2.12 shows the valence band edge of two mirror periods with abrupt interfaces (dotted line) and with linearly graded interfaces (solid line). The grading length in the Figure was chosen as $30\,nm$. Such a compositional grading can easily be achieved during MOVPE growth by ramping the gas flows of the trimethyl-gallium and trimethyl-aluminum sources. The result of the *SimWindows* simulation shows that the barrier height is reduced from $330\,meV$ to $44\,meV$ in the case of graded interfaces. Thermal emission over this barrier becomes much more likely and therefore the electrical resistance of the mirror will largely be reduced.

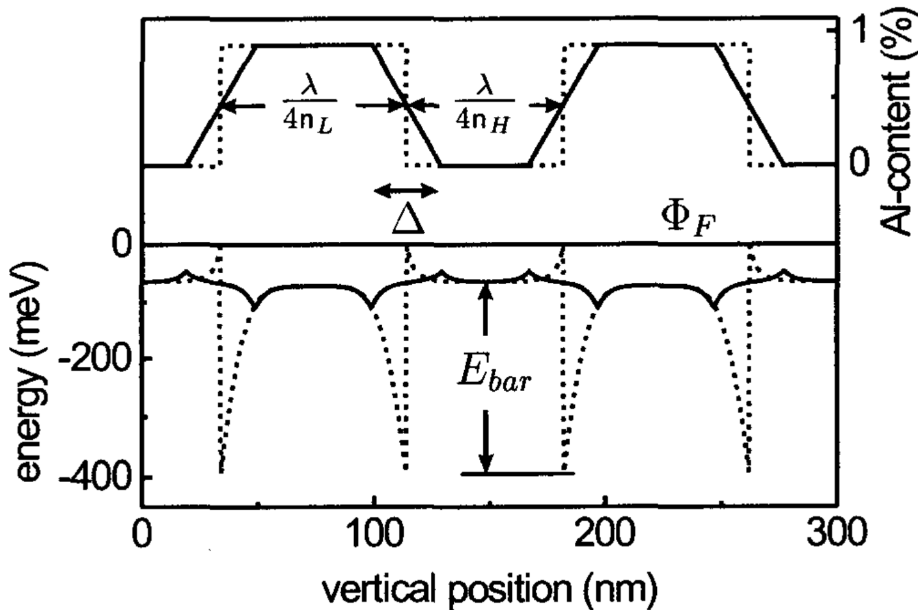


Figure 2.12: Aluminum content and valence band edge for two mirror periods of a non-graded (dotted) and a graded (solid) DBR. The length of one mirror period is $148\,nm$, the grading length $d_{grad} = 30\,nm$ and the acceptor concentration is $10^{18}\,cm^{-3}$.

2.1.4 Laser efficiency

High laser efficiencies are of course desirable for low power applications. Besides the simple energy budget there are a number of other interesting advantages of highly efficient VCSELs: They allow to obtain high optical output powers [14] and high single transverse mode powers [15]. The wavelength shift with current is low, since little ohmic heat is generated. Furthermore, the reliability is enhanced if a device can be operated at a relatively low injection current, and if the device resistance produces little heat [49]. Finally, the high-speed modulation properties of a VCSEL may be improved by a high efficiency: With a low electrical resistance R, the time constant $\tau = RC$, where C is the parasitic capacitance of the laser, is short.

In this section the terms used to describe the laser efficiency are introduced. The most important parameters are the *differential efficiency* η_d and the *wall-plug efficiency* η_{WP}. The effect of different numbers

of mirror periods in the top outcoupling mirror is investigated with a series of experiments.

Differential efficiency

The differential efficiency of a laser is defined as the increase in light output, due to an increase in the drive current. If only the light which is coupled out through the top mirror is collected, the differential efficiency is

$$\eta_{d,top} = \frac{q}{h\nu}\frac{dP_{top}}{dI} \tag{2.21}$$

The prefactor with the photon energy $h\nu$ and the electric unit charge q normalizes the differential efficiency such that $\eta_{d,top} = 1$ if every injected electron produced a photon. Therefore, $\eta_{d,top}$ normally lies between 0 and 1. The differential efficiency is sometimes also called 'quantum efficiency' to take into account the quantum nature of the photon generation, or 'slope efficiency' because it corresponds to the slope of the power vs. current curve.

In an ideal top-emitting VCSEL, every injected carrier would recombine into the lasing mode, and the generated photon would be coupled out through the top mirror, giving a value of $\eta_{d,top} = 1$. In a real laser, several loss mechanisms lead to a reduction of $\eta_{d,top}$: First of all, only a fraction η_i of the injected carriers will recombine into the lasing mode, as discussed in the last section.

Secondly, some of the generated photons will be reabsorbed or scattered away inside the cavity. The fraction of outcoupled photons is found by dividing the mirror outcoupling loss

$$\alpha_m = \frac{1}{L_{eff}} \ln\left(\frac{1}{\sqrt{R_{top}R_{bot}}}\right) \tag{2.22}$$

by the total cavity losses. In this equation the lossless mirror reflectivities are used. L_{eff} is the total effective cavity length, given by

the sum of the top and bottom mirror penetration depths $l_{eff,top}$ and $l_{eff,bot}$ and the cavity length l_{cav}. The total cavity loss is the sum of the mirror loss α_m plus absorption loss α_i, which is given by

$$\alpha_i = \frac{1}{L_{eff}}(l_{eff,top}\alpha_{i,top} + l_{cav}\alpha_{i,cav} + l_{eff,bot}\alpha_{i,bot}) \tag{2.23}$$

The material absorption coefficients $\alpha_{i,x}$ in the different laser sections are generally different. With mirror doping levels of $2 \cdot 10^{18}\, cm^{-3}$, $l_{eff} = 450\, nm$, $l_{cav} = 280\, nm$ and free carrier absorption coefficients taken from Equation 2.7, the internal loss amounts to $10\, cm^{-1}$. The ratio between outcoupled photons to those generated in the active material then becomes

$$\eta_{out} = \frac{\alpha_m}{\alpha_m + \alpha_i} \tag{2.24}$$

A high efficiency VCSEL must be designed so that the internal absorption α_i is small in comparison to α_m, so that this fraction is close to unity.

The last factor which reduces the differential efficiency is the asymmetry factor F_{top}. This factor gives the ratio of photons coupled out through the top mirror, divided by the number of photons coupled out through both mirrors [29]:

$$F_{top} = \frac{(1 - R_{top})e^{-2\alpha_{i,top}l_{eff,top}}}{(1 - R_{top}) + \sqrt{\frac{R_{top}}{R_{bot}}}(1 - R_{bot})} \tag{2.25}$$

Again, the reflectivities calculated for lossless mirrors must be inserted. A high value of F_{top} is obtained if the mirrors are designed asymmetrically, such that $R_{bot} \gg R_{top}$.

Collecting the different terms, the differential efficiency of the laser becomes:

$$\eta_{d,top} = \eta_i F_{top}(\frac{\alpha_m}{\alpha_i + \alpha_m}) \tag{2.26}$$

The first term in this equation depends only on the cavity design and was optimized in the last section. Its measured value is $\eta_i = 0.84$.

The other two factors depend on the mirror design. With the chosen values of doping levels, *Al* content in the mirrors and interface gradings, the last free parameter in the mirror design is the number of mirror periods. Figure 2.19 shows the differential efficiency calculated as a function of the number of mirror periods in the top DBR, assuming 30 mirror periods in the bottom DBR. This higher number of periods in the bottom mirror keeps the last term in Equation 2.26 close to unity as long as the top mirror consists of less than about 22 periods (see Figure 2.19). The calculation was performed with a transmission matrix program. Besides the differential efficiency, the two terms on the right of Equation 2.26 are also plotted.

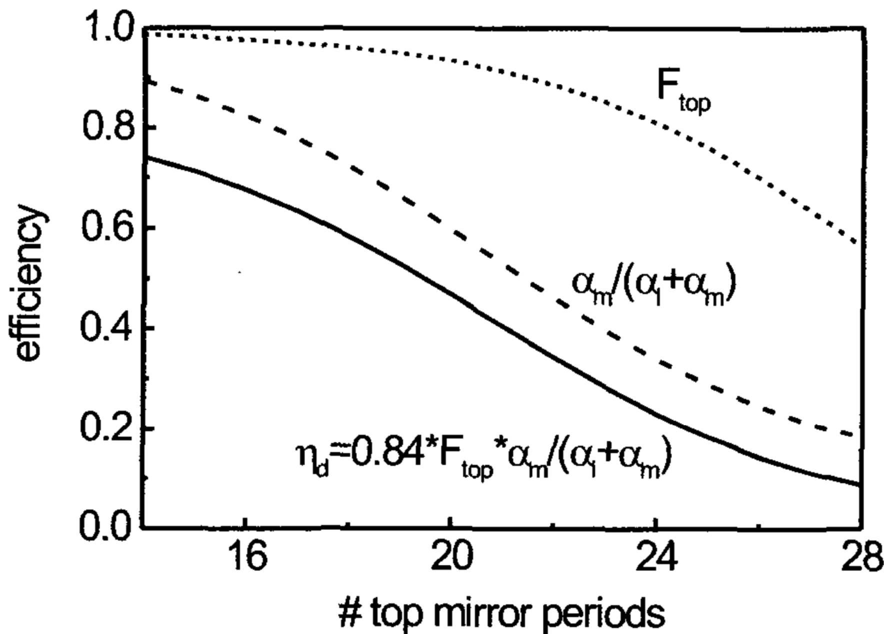


Figure 2.19: Calculated differential efficiency as a function of the number of mirror periods in the top DBR (solid line). The contributions of the asymmetry factor F_{top} (dotted line) and $\alpha_m/(\alpha_i+\alpha_m)$ (dashed line) are plotted separately as well.

While the asymmetry term F_{top} is close to unity with an appropriately large number of mirror periods in the bottom mirror, the third term in Equation 2.26 degrades the differential efficiency significantly.

With the assumed absorption levels, the top mirror has to have less than 17 periods to keep the factor $\alpha_m/(\alpha_i + \alpha_m) > 0.8$. This leads to relatively high threshold currents. The alternative would be to further reduce the internal absorption by using an improved dopant profile in the mirror, as discussed in Section 2.1.3.

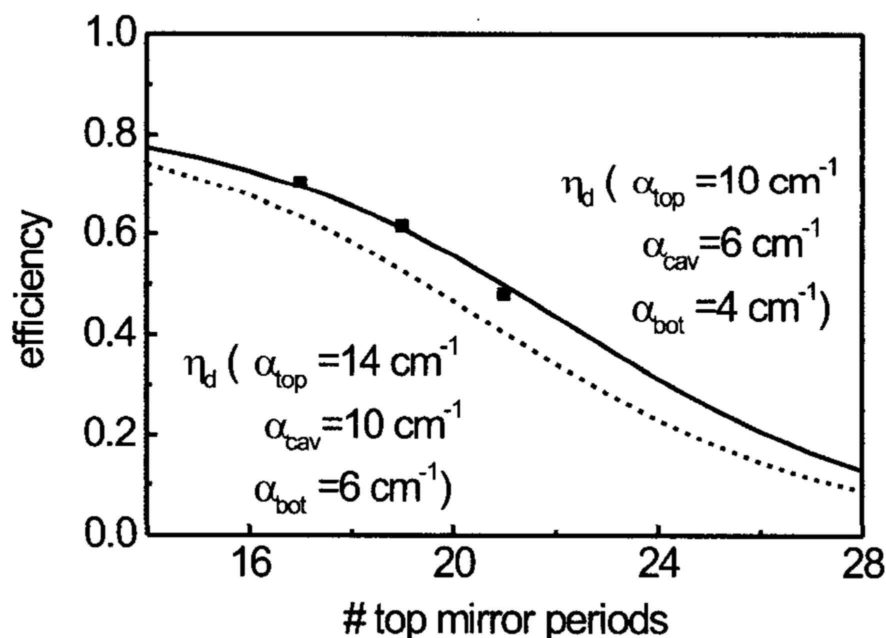


Figure 2.20: Experimentally determined differential efficiencies (squares) of VCSEL structures with 17, 19 and 21 mirror periods in the top mirror. The efficiencies were evaluated in oxidized VCSELs with an oxide aperture radius of $5\,\mu m$. For comparison, theoretical curves assuming absorption coefficients corresponding to the design doping levels (dotted line), and 40 % below the design values (solid line) are also shown.

Three VCSEL structures with the cavity design B were grown with a different number of periods in the top mirror (m_{top} = 17, 19, 21). The bottom mirror always had 30 mirror periods. Selectively oxidized VCSELs from the three structures were processed, and the differential efficiencies of relatively large VCSELs were compared. A $10\,\mu m$ oxide diameter was chosen so that scattering losses should be neglectable (see Section 2.2.2). Figure 2.20 shows the measured values of the

differential efficiencies. For comparison with theory, the figure also shows the calculated efficiency, similar to Figure 2.19. The theoretical curve which uses the absorption coefficients corresponding to the design doping levels falls well below the measured efficiencies. The measurements of the electrical mirror conductivities in Section 2.1.3 revealed that the doping levels in the VCSELs are as much as 40 % lower than designed. Assuming that the doping levels are in fact 40 % lower than designed, one obtains lower absorption losses and subsequently a higher efficiency, which is also plotted in Figure 2.20 as a solid line. As can be seen, the assumption of lower doping levels is well supported by this measurement.

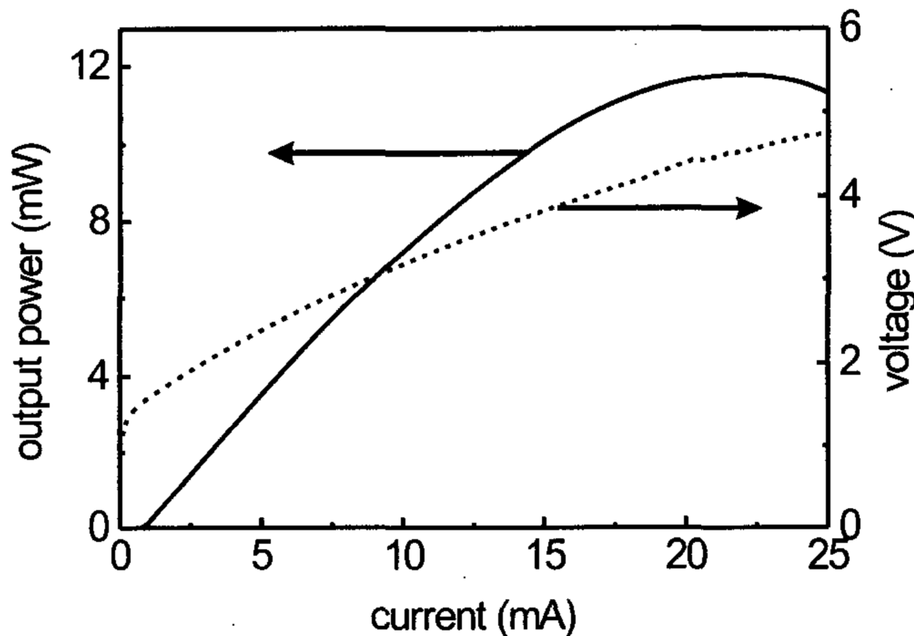


Figure 2.21: Typical power out versus current curve of a VCSEL with 19 periods in the top mirror. The threshold current density of this device with an oxide aperture radius of 5 μm is 1 kA/cm^2.

The structure with 17 periods in the top mirror has a differential efficiency of 71 %. This is among the highest values reported [50]. It should be noted, that the high differential efficiencies are obtained with lasers, which still have a relatively low threshold current density

of around $1\,kA/cm^2$, as shown in the example of a light vs. current curve (LI-curve) in Figure 2.21.

Wallplug efficiency

The overall conversion efficiency from electrical input power to optical output power P_{out} of the laser is called the wallplug efficiency η_{WP}:

$$\eta_{WP} = \frac{P_{out}}{I \cdot V} \tag{2.27}$$

I and V are the drive current and voltage respectively. A high wallplug efficiency requires a low threshold current, a high differential efficiency and a low voltage drop across the device, all at the same time.

The fraction of the electrical input power which is not emitted as laser light will result in device heating. This heat reduces the optical gain and shifts the wavelength alignment between gain and cavity mode of the VCSEL. The result is a reduction of both differential and wallplug efficiency with increasing injection current. This so-called thermal roll-over can be observed in the LI-curve shown in Figure 2.21, which becomes non-linear for currents above $\sim 5\,mA$ and reaches a maximum at $22\,mA$.

Figure 2.22 illustrates the current dependence of the wallplug efficiency of devices with 17, 19 and 21 periods in the top mirror. A smaller number of mirror periods reduces the reflectivity in the outcoupling mirror, and leads to an increased wallplug efficiency. However, when the reflectivity of the outcoupling mirror is reduced too much by using fewer mirror pairs, the VCSEL threshold condition cannot be fulfilled and the device will not work as a laser anymore. We did not observe this case, since 17 mirror periods was the lowest number used in our structures. The 17 mirror period structure did have an increased threshold current in comparison with the other VCSELs (see Figure 2.22). As a consequence, in a small current range

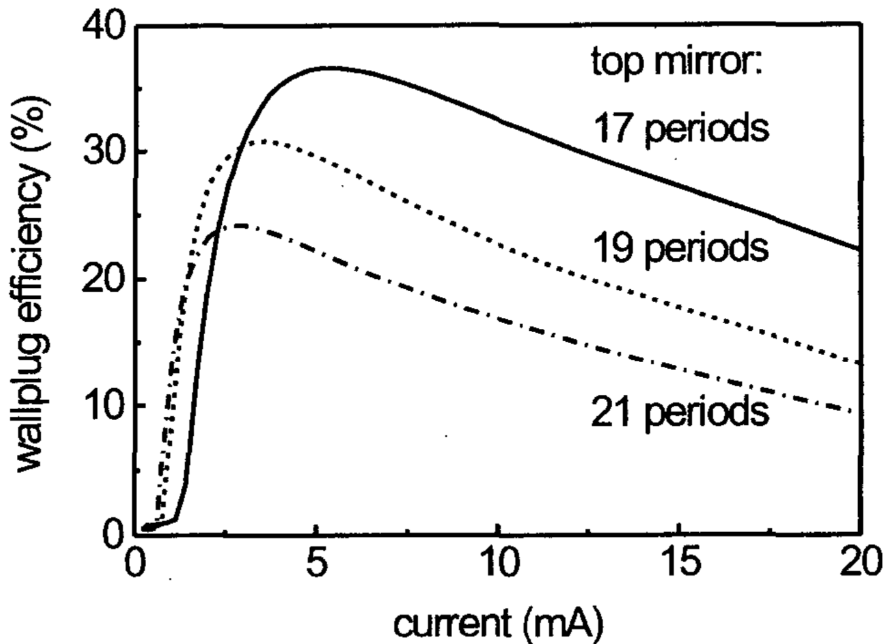


Figure 2.22: Wallplug efficiencies of devices with 17, 19 and 21 periods in the top mirror, and an oxide aperture radius of $5\,\mu m$. The maximum values are obtained at relatively low injection currents, where the output power does not suffer from thermal roll-over. The peak values of the wallplug efficiency are 36 %, 31 % and 24 % for the three different designs.

above threshold, the wallplug efficiency for the high mirror reflectivities is higher.

The highest measured wallplug efficiency of 36 % is not quite as good as the best values reported in the literature of 50 – 57 % [13, 51]. The devices described in these publications both use carbon as p-type dopant, while our devices used magnesium. Carbon has a lower diffusivity and higher solubility in the host crystal than magnesium [52] and therefore allows to dope the reverse biased heterointerfaces in the mirror to a higher level. Since the positions of these interfaces coincide with optical field nodes, a higher doping level does not increase the absorption and has therefore no adverse effect on the efficiency. A higher doping level will thus lower the device resistance without

a penalty. As a second approach, the mirror doping levels could be reduced near the cavity where the optical field has a high intensity. This would reduce absorption and lead to a lower threshold, while the effect on the mirror resistance is minor. The higher wallplug efficiencies reported in [13] and [51] are explained mainly by these two improvements.

Chapter 4: Current confinement and lateral hole spreading

4.1 Introduction

One of the main obstacles for the fabrication of electrically injected GaN-based VCSELs is related to the poor *p*-type doping characteristics. The conductivity of *p*-doped GaN is relatively low due to the large ionization energy of the magnesium impurities and the low hole mobility. Common injections schemes for GaAs-based VCSELs contemplate the use of conductive DBRs with and without current confinement layers (figures 4.1 (a)-(b)) or the use of annular intra-cavity contacts in combination with one or two current confinement layers (figure 4.1 (c)) [1].

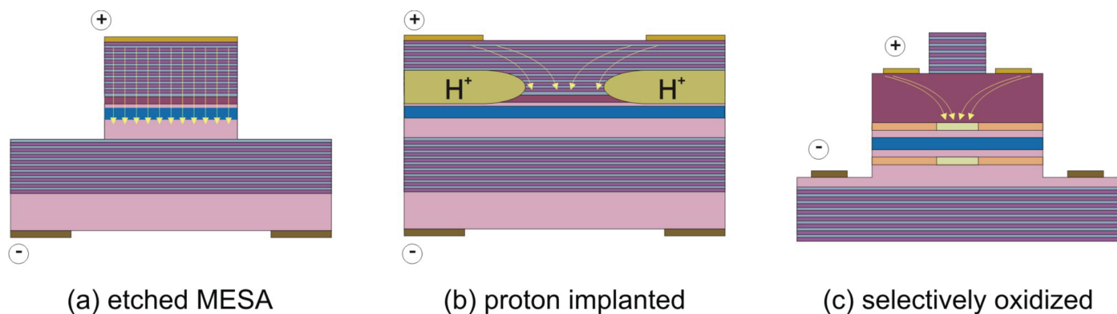


Figure 4.1: Schematic of some common injection and current confinement schemes employed in GaAs-based VCSELs. (a) Etched mesa (bottom emitting): current confined to the mesa width: conduction through the mirrors. (b) Proton implanted (top or bottom emitting): current confined by the semi-insulating region formed after the implant; conduction through the mirrors. (c) Selectively oxidized (top or bottom emitting): current confinement area defined through the oxidation of sacrificial layers; current conducted laterally along the contact layers.

Although considerable progress has been made in the realization of high quality GaN based distributed Bragg reflectors (DBRs) [2-5], efficient carrier injection into the active region still remains an obstacle. While *n*-type doping of nitride-based DBRs has already been demonstrated [6, 7] an efficient *p*-type doping

cannot be reached, precluding thus the possibility to inject carriers directly through DBRs. For this reason a cavity design with intra-cavity contacts has to be used. Unfortunately, the relatively poor lateral hole spreading into the *p*-type GaN layer makes the bare annular contact geometry inefficient for achieving current injection in the central part of the devices as emission is only localized under the contact.

The most common solutions to overcome these problems consist in using either a semitransparent contact, generally made of ITO, or a tunnel junction (TJ). Nitride-based vertical light emitting diodes (LEDs) including one of these features have already been demonstrated [8-10] but, so far, no lasing condition has been reached using such solutions.

The use of a semitransparent spreading layer like ITO is detrimental in terms of absorption losses. Margalith *et al.* measured an absorption coefficient of ~660 cm^{-1} at 420 nm for a 25 nm thick ITO layer [11]. Although this value is low compared to that of semitransparent metallic layers, it should prevent a VCSEL structure from reaching lasing.

On the other hand, different groups have already succeeded in integrating a TJ in LED structures, but problems related to a non uniform current injection still remain. In such TJs, the influence of local composition and doping inhomogeneities seems to be a critical issue [10]. Moreover, although an improvement of the hole spreading has been demonstrated by using these solutions, none of them includes a current confinement layer. The primary purpose of these structures is to obtain a VCSEL having limited lateral extent without introducing unwanted losses, so that relatively small devices, with reasonable electrical characteristics in continuous wave (CW) operation, can be fabricated.

This chapter is focused on this last point. An electrical injection design suitable for VCSEL structures is presented, where a *p*-type ring contact geometry is adopted. The current confinement is achieved by inserting an AlInN interlayer used as carrier confinement layer after a lateral oxidation process [12]. Such design allows reaching current densities of the order of 20 kA/cm^2 in the active region under cw operation. In the end some considerations on the improvement of the hole lateral spreading will be done.

Oxide VCSELs - fabrication

In an oxide VCSEL process, a very thin, buried AlAs layer is laterally oxidized from an exposed mesa side wall to a depth of around 10 μm. With a typical oxide layer thickness of 25 nm, this means that the oxide extends 400 times deeper into the material than the width of the exposed surface. Figure 3.1 illustrates this large aspect ratio. An SEM photograph of a cleaved mesa containing many oxide layers is shown in Figure 3.3.

The oxide is a good electrical insulator, and thus an electrical current in the finished device is confined to the oxide aperture in the center of the VCSEL mesa. At the same time, the low refractive index of the oxide ($n \approx 1.55$ [61, 62, 63]) serves as a strong optical waveguide for the laser mode.

The oxidation process is carried out in a wet hot ambient, inside

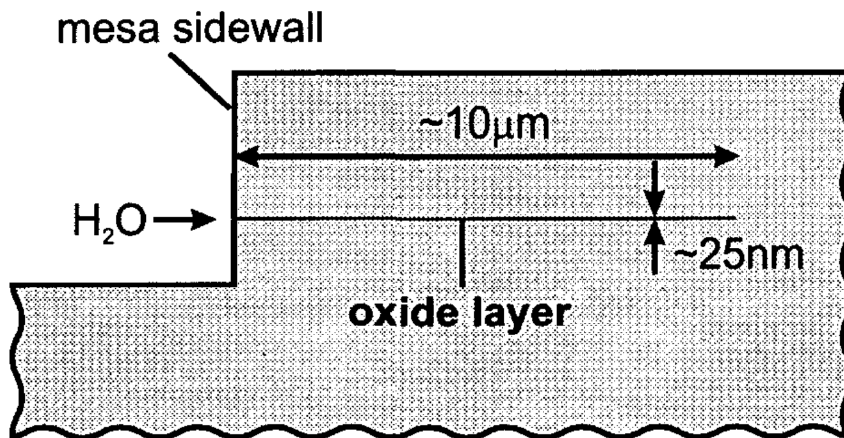


Figure 3.1: The lateral oxidation proceeds into a thin, buried layer, from the side of an etched mesa. The H_2O processing gas has to reach the reaction front by moving in through the already oxidized material. The plot illustrates the relative extents of oxidation depth and oxide layer thickness.

an oxidation furnace. The beginning of this chapter summarizes the oxidation chemistry, to facilitate an understanding of the necessary process environment. In the second part, the oxidation setup built is described, and the influence of various process parameters on the oxidation rate is presented. The third part describes how this oxidation process was incorporated into the fabrication of VCSELs. The final part is devoted to the reliability of VCSELs with different oxide layer designs.

3.1 Oxidation chemistry

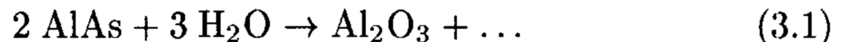
The success of silicon in the integrated-circuit technology is largely based on the ability to grow a stable native oxide on Si with relatively easy methods. Thermal oxidation at 900 to 1200° C with oxygen (dry oxidation) or with water vapor (wet oxidation) forms

amorphous SiO_2 on a Si surface. This oxide may be used for masking in implantation steps, and the high resistivity of the material is used to form thin gate oxides in metal-oxide-semiconductor field effect transistors.

Obtaining a similar robust oxide for III-V compound semiconductors such as $GaAs$ was pursued for decades without success. Aluminum bearing III-V compounds such as $AlAs$ are known to oxidize at room temperature in an uncontrolled manner, particularly in moist environments. However, the oxide produced in this environment is very fragile and thus unusable for devices. The same is true for the oxide formed in an early attempt to control the oxidation process of $AlAs$ in an $O_2 : H_2O : N_2$ atmosphere at elevated temperatures [64].

The break-trough came in 1990, when a research team at the University of Illinois attempted an accelerated hydrolyzation oxidation of $AlAs$, by passing *pure* water vapor ($H_2O : N_2$) over it in a furnace at $400\,°C$. In contrast to all previous attempts, these experiments produced a smooth and dense native oxide on $AlAs$ [11]. The oxide was found to be stable, and even to protect the underlying semiconductor material from environmental degradation [62]. The superior characteristics of this oxide indicate that the material must be different from the oxide produced in an O_2 containing process environment. In fact, the oxide produced in the wet oxidation may very well be different, as there exist many different phases of aluminum oxides and hydroxides [65].

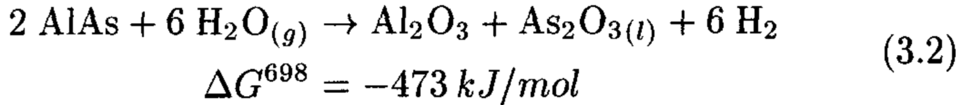
Since N_2 acts only as inert carrier gas in the process, the wet oxidation chemistry must be of the form



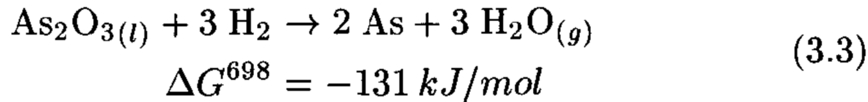
$$2\,\mathrm{AlAs} + 3\,\mathrm{H_2O} \rightarrow \mathrm{Al_2O_3} + \ldots \qquad (3.1)$$

where H^+ from the H_2O molecule is the oxidizing agent (and not the oxygen atom, which is already in a -2 oxidation state before the reaction!). This incomplete formulation of the chemical reaction cannot explain, why admixture of O_2, which is a much stronger oxidizer than H_2O, suppresses the reaction [66]. The observation of As_2O_3

as an intermediate reaction product motivated the following interpretation [67]: The oxidation reaction involves two partial reaction steps:



$$2\ \mathrm{AlAs} + 6\ \mathrm{H_2O}_{(g)} \rightarrow \mathrm{Al_2O_3} + \mathrm{As_2O_3}_{(l)} + 6\ \mathrm{H_2} \quad \Delta G^{698} = -473\, kJ/mol \tag{3.2}$$



$$\mathrm{As_2O_3}_{(l)} + 3\ \mathrm{H_2} \rightarrow 2\ \mathrm{As} + 3\ \mathrm{H_2O}_{(g)} \quad \Delta G^{698} = -131\, kJ/mol \tag{3.3}$$

Both of these steps are thermodynamically favorable at $425\,°C$, as they lower the Gibbs free energy G. Admixture of O_2 to the processing gas consumes the intermediate H_2, and thus suppresses the formation of volatile As (or AsH_3, which may be produced by further reaction with H_2). In this case, the As_2O_3 is stuck in the oxide material, and thus seals the oxidation front from the process gas. The reason why dry oxidation doesn't work lies actually not in the oxidation chemistry, but in the missing transportation of the reaction products.

While the process strongly favors $AlAs$ for oxidation, it also oxidizes $Al_xGa_{1-x}As$ with high Al content at a slower rate. $GaAs$ is stable and cannot be oxidized with H_2O at the temperatures investigated. By replacing Al with Ga in the reaction 3.2, the change in Gibbs free energy becomes $\Delta G^{698} = +11kJ/mol$ [67], which shows that such a process is not thermodynamically favorable at $425\,°C$.

The microstructure of the oxide material was extensively studied [68, 69]. The stoichiometry of wet oxidized $AlAs$ is Al_2O_3 [70], which is originally formed as an amorphous solid solution. Under hot temperature dry annealing, or when the material is exposed to an electron beam, the solution can be transformed into crystalline grains of $\gamma - Al_2O_3$ [70, 71].

Upon oxidation, the $AlAs$ layers typically contract in thickness by about 10 % [69, 72]. This causes strain, which may lead to mechanical instability and reliability problems of devices [73].

3.2 Oxidation process

3.2.1 Experimental setup

In principle, the wet oxidation of high Al-content $AlGaAs$ is a relatively simple procedure. The difficulties lie in the strong temperature dependence of the process, and the fact that minute amounts of O_2 in the furnace can bring the oxidation to a halt. Therefore, a good control on these parameters is required for the establishment of a uniform, accurate, and reproducible oxidation process.

The setup is shown in Figure 3.2. The furnace consists of a 3 inch diameter quartz tube, approximately 1.5 m in length. Three sections of heating wire are coiled around an outer tube, inside which the actual furnace resides. The temperature in the three sections is measured and stabilized by thermocouples and standard PID controllers. The rather large furnace design and the three individual heating sections facilitate an accurate and uniform temperature control in the center of the furnace.

The N_2 carrier gas is preheated and mixed with H_2O in a controlled evaporator and mixing (CEM) system. This system controls the supply of H_2O with a liquid flow meter and a microprocessor controlled valve, while the N_2 flow is stabilized with a mass flow controller. The processing gas mixture enters the furnace from the rear end, reacts with the sample in the furnace, and exits through the exhaust located near the front of the furnace, where the H_2O is condensed in a vessel. A lid covering the furnace front can be opened for sample insertion. The wafer to be oxidized is mounted on a aluminum heat spreading plate, which is inserted into the furnace with a sample holder made out of quartz glass.

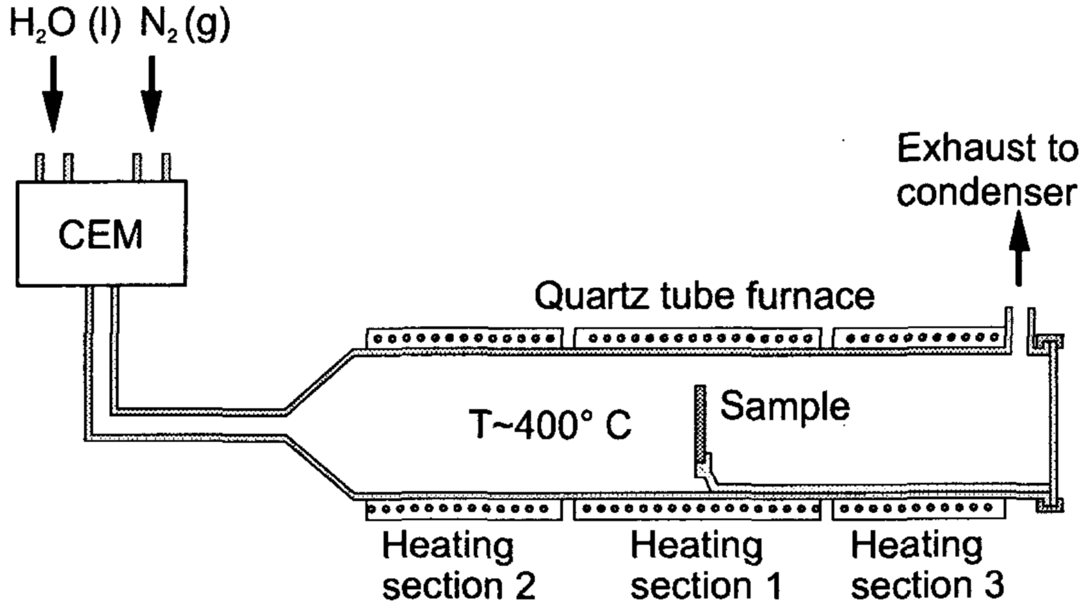


Figure 3.2: Furnace design used for the oxidation experiments. A controlled evaporator and mixing (CEM) system is used to produce the hot water vapor.

3.2.2 Process parameters

Just as in *Si* oxidation technology, the dependence of the oxidation depth d_{ox} on process time t can be written as [74]

$$d_{ox}^2 + Ad_{ox} = Bt \tag{3.4}$$

B is related to the diffusion constant of the reactants moving through the oxide, and B/A is associated with the interfacial reaction rate. For thin layers, where the process is reaction rate limited, the oxidation depth follows the linear relation

$$d_{ox} = (B/A)t \tag{3.5}$$

On the other hand, for large oxidation depths, Equation 3.4 results in a square root dependence of d_{ox} vs. time. The process is then

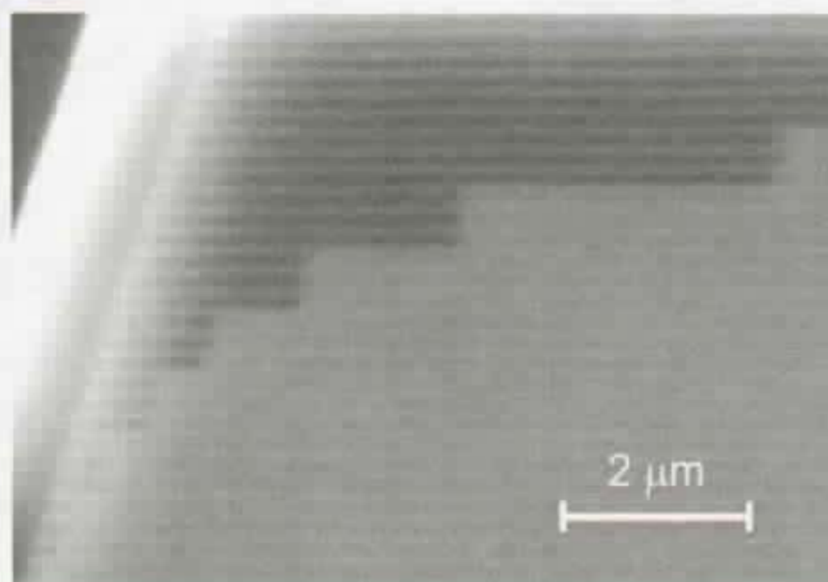


Figure 3.3: SEM picture of cleaved oxidation test sample. The structure contains $AlGaAs$ layers with different Al contents, which are oxidized from the mesa edge to different depths. The oxide appears black in the SEM, and the light cap covering the mesa edge is Si_3N_4, which was deposited after oxidation.

limited by diffusion of the reactant gas through the already oxidized material.

Figure 3.4 a) shows a measurement of the lateral oxidation depth versus processing time in a thin $AlAs$ layer. The oxidation depths were measured on cleaved test samples in the SEM, as shown in Figure 3.3. The two parameter oxidation law 3.4 describes the measured data very well, with linear relation 3.5 being a good approximation for oxidation depths up to about $30\,\mu m$. This shows that the chosen parameters lead to a reaction rate limited process for the oxidation depths we are interested in. The retarded start of the oxidation after sample insertion is simply due to the sample temperature: The sample, which is mounted on the initially cold heat spreading plate, takes

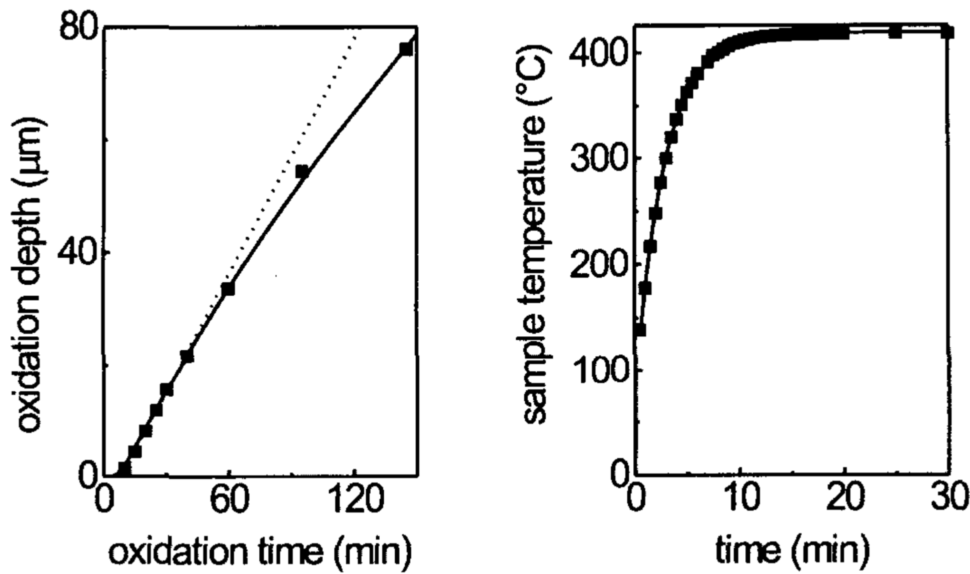


Figure 3.4: a) Measured oxidation depths in a 50 nm thick $AlAs$ layer after different oxidation times at 420 °C. The gas flows are 0.5 l/min N_2 and 20 g/h H_2O. The late start of the oxidation process is due to the slow temperature equilibration of the sample holder after insertion into the furnace. b) shows the temperature measured on the sample holder after insertion into the furnace.

a few minutes to reach the furnace temperature where the oxidation reaction sets in.

The linear oxidation rate of $AlGaAs$, which is simply called r in the following ($r = B/A$), depends on many parameters. First of all, the dependence on the Al content in an $Al_xGa_{1-x}As$ layer was measured in the test sample shown in Figure 3.3. This sample contains 50 nm thick layers with different Al composition, ranging from $x = 0.7$ to $x = 1$. The results are summarized in Figure 3.5. The process is highly selective for high Al compositions, with a two orders of magnitude slower oxidation rate for $Al_{0.85}Ga_{0.15}As$ than for $AlAs$. This extremely high selectivity can be used to oxidize only a selected

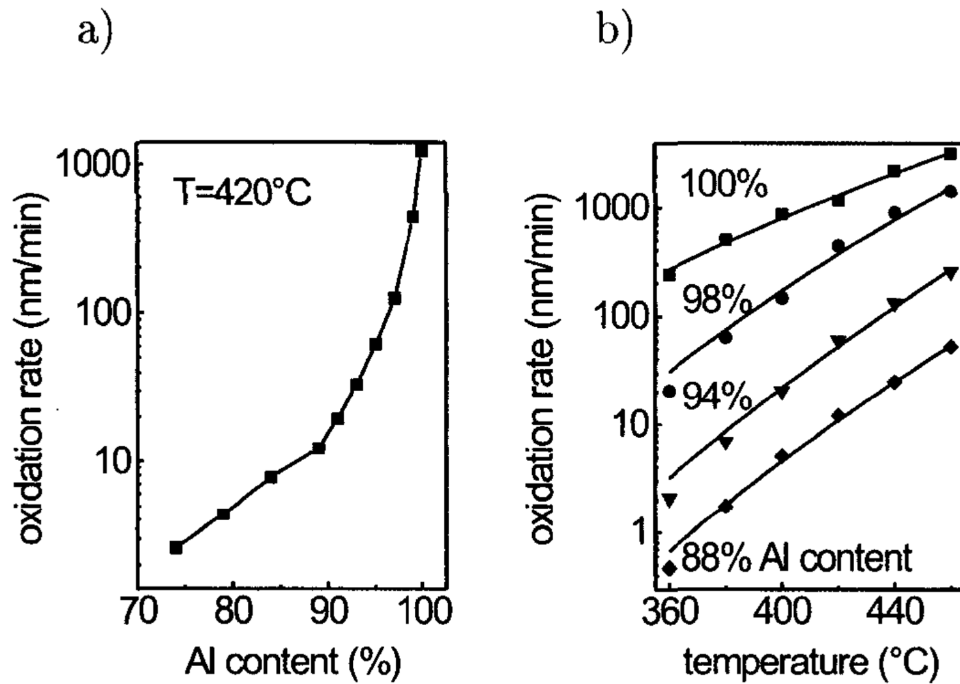


Figure 3.5: a) Oxidation rate dependence on Al content in $Al_xGa_{1-x}As$, at $T = 420\,°C$ and a gas flow of $0.5\,l/min\ N_2$ and $20\,g/h\ H_2O$. b) Temperature dependence of the oxidation rate for a few different $Al_xGa_{1-x}As$ compositions. The lines show an Arrhenius type linear fit.

layer in a complicated multilayer structure.

The temperature dependence of the oxidation rate $r(T)$ follows an Arrhenius law over the investigated temperature range:

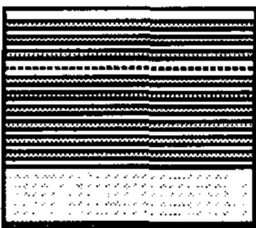
$$r(T) = r_0 \cdot exp(-\frac{E_a}{kT}) \tag{3.6}$$

with a constant r_0 and an activation energy E_a. An Arrhenius fit to the measured temperature dependence of the oxidation rate for different Al-compositions is shown in Figure 3.5 b). The activation energy E_a is approximately $1.7\,eV$ for layers up to $\sim 97\,\%$ Al content, and then drops to $1\,eV$ for pure $AlAs$. Therefore, the selectivity of the process is reduced for higher temperatures.

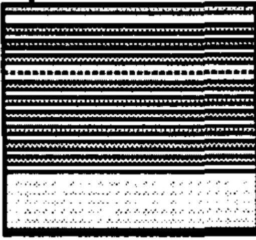
In summary, with an abundant H_2O supply, the oxidation rate is only a function of temperature and the layer structure. By accurately controlling the sample temperature and the process time, the oxidation depth becomes very uniform across the sample and also reproducible. Figure 3.7 illustrates the uniformity of the process across a full 2 inch wafer. Part a) of the figure shows the oxidation depth measured directly in the SEM, and b) shows the uniformity of the obtained VCSELs by plotting the threshold current distribution of more than 13 thousand measured devices.

3.3 Fabrication of selectively oxidized VCSELs

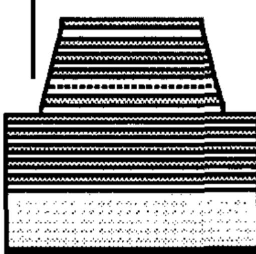
The epitaxial layer structures used in this work were grown with MOVPE. After growth, the wafer has to be processed into laser devices. This fabrication process is described very briefly in the following with the help of schematical drawings, for the case of the oxidized VCSELs.



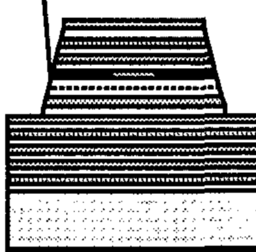
1) A $GeAuNiAu$ n-contact is evaporated on the backside of the wafer. The contact is annealed at $420\,°C$ in a rapid thermal annealer (RTA) for 30 seconds. The metalization is carried out prior to oxidation, even though the measured contact resistance deteriorates slightly from 2 to $3 \cdot 10^{-6}\,\Omega cm^2$ during the subsequent oxidation. The reason is that the RTA step sometimes leads to mechanical instability of oxidized mesas, when done after the oxidation.



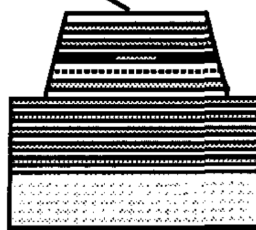
2) A Si_3N_4 layer is deposited by plasma enhanced vapor phase epitaxy (PECVD) on the front side of the structure, to protect the laser surface during the oxidation process. Without this protection layer, the oxidation produced irregular spots on the laser surface.



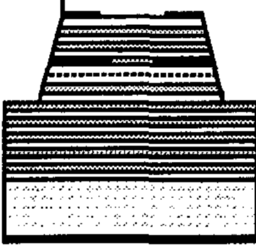
3) A dry etch using a BCl_3 plasma in an electron cyclotron resonance (ECR) reactor is used to define the circular VCSEL pillars. The etch depth is sufficiently deep to laterally expose the buried $AlAs$ layer used for oxidation.



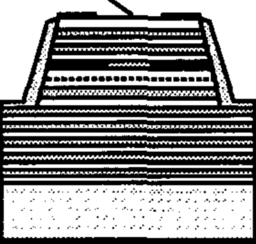
4) The buried $AlAs$ layer in the sample is laterally oxidized at $420\,°C$ in a $H_2O : N_2$ ambient, as described in the second part of this chapter.



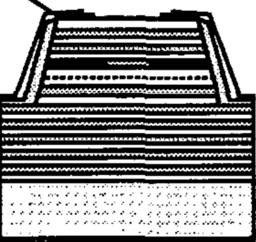
5) The Si_3N_4 protection layer is removed with a reactive ion etch (RIE) etch, using CF_4.



6) A *PtTiPtAu* *p*-type *ring contact* is evaporated on top of the mesa, using image reversal resist and a metal lift-off process. Before evaporation of the metals, a short $NH_3 : H_2O$ dip is used to clean the semiconductor from any surface oxides. The contact resistance of the non-alloyed, ohmic *p*-contact was measured to be about $10^{-5}\,\Omega cm^2$.



7) A Si_3N_4 *isolation layer is deposited on the* device surface with a PECVD process. This isolation layer is then re-opened on top of the mesas by reactive ion etching.



8) The final processing step is evaporation of *TiPtAu* metal, using image reversal resist and a lift-off process. This metal layer is used to define bond pads, and to wire these pads with the p-contact ring on top of the mesas.

4.2 The AlInN selective anodic oxidation

Processing on nitride compounds involves fundamental processing drawbacks, due to their enhanced hardness and chemical inertness compared to other III-V semiconductors. One important example is represented by the selective oxidation of Al-rich layers [13, 14].

This process is a standard technique adopted for the AlAs/GaAs alloys [15]. It allows successful current confinement schemes in GaAs-based VCSELs. The selective oxidation technique is based on the insertion of AlAs or Al-rich AlGaAs layers in the device structure during the epitaxial growth. No degradation of the structural quality is occurring, since AlAs is nearly lattice-matched to GaAs. Mesa structures are then etched in order to give access to these sacrificial layers from the sidewalls. Al(Ga)As layers are then oxidized in wet atmosphere at temperatures around 450°C and converted into an aluminum-oxide (AlO_x) while the other layers are unaffected by the process [16]. The oxidation depth in the lateral direction can be precisely controlled. The oxidized layers are electrically insulating and thus can be used to define small current apertures for the electrical confinement in GaAs based optoelectronics devices [17].

As already seen in previous chapters, among III-nitrides, Al-rich AlGaN alloys exhibit a significant lattice mismatch to GaN and induce tensile strain in the structure. This limits their use as sacrificial layers for selective oxidation processes since the in-built strain could lead to a degradation of the structural quality or even to the damage of the device. The alternative solution of using LM AlInN layers for the oxidation is considered here. In any case, the wet oxidation technique developed for Al(Ga)As layers does not lead to similar results for AlInN layers, even at temperatures as high as 900°C.

The procedure developed allows selective anodic oxidation of such LM AlInN layers [12]. Using this technique, lateral oxidation of buried AlInN layers can be achieved over several tens of micrometers. The AlInN layers are oxidized anodically in a nitrilotriacetic acid/potassium hydroxide (NTA/KOH) electrolyte.

The first step consists in inserting a LM AlInN layer into the device structure during the MOVPE epitaxial growth. Such layer has to be placed in the *n*-type side

since it is currently impossible to grow *p*-doped AlInN layers. An *n*-doped GaN buffer layer is recommended to decrease the access resistance presented by the device during the oxidation process and, consequently, the homogeneity of the oxidation itself. Also doping levels have a large impact on the applied voltage and the oxidation rate. After the growth and after the thermal Mg activation, a SiO_2 mask is deposited on the wafer and circular mesa structures, 20 μm in diameter, are etched down to *n*-GaN bottom layer (200 to 300 nm below the top surface), giving access to the AlInN layer sidewalls. Lateral anodic oxidation of AlInN is then performed in a NTA/KOH solution. The SiO_2 cap layer is maintained, to protect the top surface of the mesa, by acting like a passivation layer. Moreover current could flow through surface defects and thereby locally oxidize the AlInN layers, which is generally not desirable. At the same time the thickness of the SiO_2 cap layer has to be kept below a certain thickness in order to limit additional strain during the oxidation process. SiO2 thicknesses should be kept between 200 and 400 nm. For current access during the anodic oxidation process, a small piece of indium is alloyed to the *n*-GaN layer.

The electrolyte is prepared by dissolving the nitrilotriacetic acid (NTA) in a 0.3 M solution of potassium hydroxide (KOH). This last is used to balance the pH level of the solution. Typical pH values for the oxidation process are around 8.5. The pH and the concentration of NTA will influence the rate of oxidation as well as the oxidation/etching rate ratio.

The NTA is known to react with metals and to form with them water-soluble complexes. Because of this ability to react with metals and to form *chelate* complexes with metallic ions, it is used in many industrial applications. In the oxidation process the NTA reacts with the metallic atoms of the AlInN layer, leading to the formation of complex AlInN-O_x products.

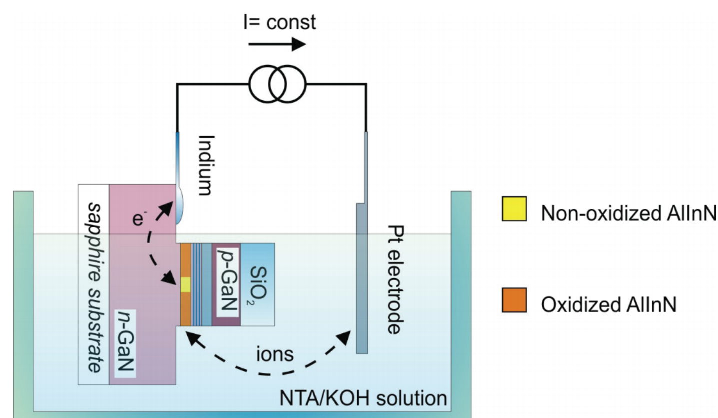


Figure 4.2: Schematic drawing of the anodic oxidation setup.

The anodic oxidation is performed at room temperature in a small beaker fitted with a platinum cathode. Typical current densities applied during the process ranges from 3 to 20 μA/cm^2. A schematic of the oxidation setup is given in figure 4.2.

The voltage drop between the two electrodes is normally between 3V and 10 V. Depending on the semiconductor structure and resistivity, this value may be higher. During the oxidation, an increase of the voltage is observed. The latter is due to the progressive increase in the length of the formed oxide. The oxidation rate ranges from 5 to 20 μm/hour. Main influencing factors are the applied current density, the thickness of the AlInN layer and the characteristics of the electrolyte. Moreover the doping levels in the structure and the presence of defects may also play a role. The most important feature of the process is its selectivity, keeping the surrounding GaN layers unaffected. The possible effects of the anodic oxidation process on the structures are shown in figure 4.3.

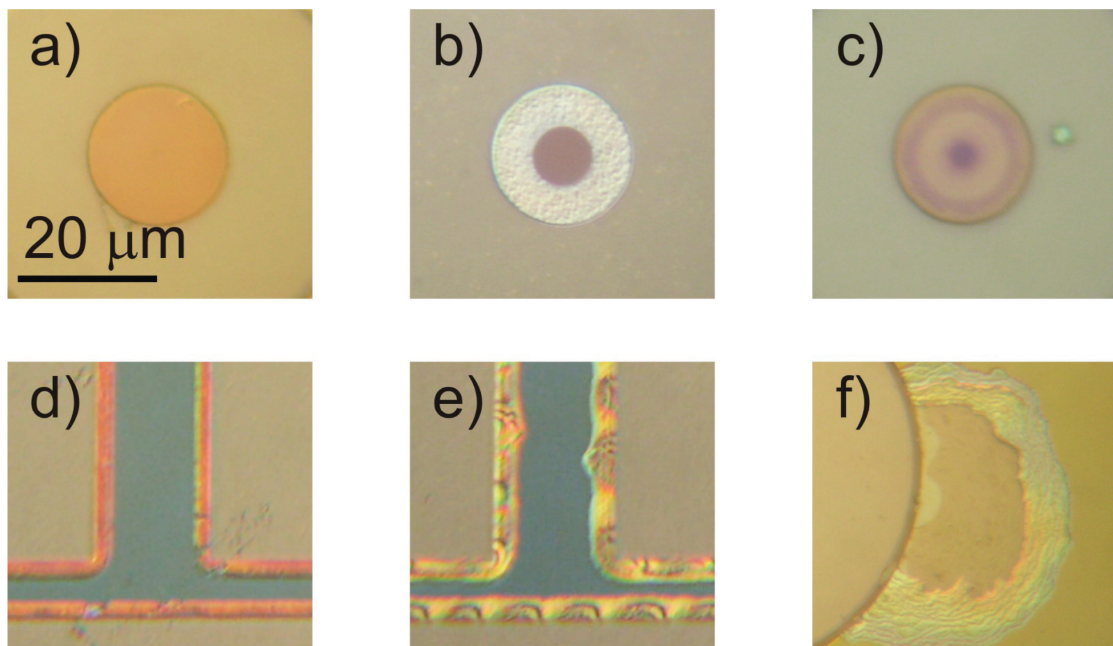


Figure 4.3: Microscope images showing the effects of the anodic oxidation process on structures including an AlInN layer. (a) Mesa structure (20 μm in diameter) before the lateral oxidation process. (b) Mesa structure after a process carried out under etching conditions. (c) Mesa structure after a process carried out under oxidation conditions. (d) Detail of an oxidized structure. (e) Strain effects induced by the SiO2 capping layer. (f) Lift-off of the layers above the etched AlInN layer.

Figure 4.3 a) shows an optical microscope image of a circular mesa before the oxidation process. Depending on the oxidation conditions two different results can be

obtained. High oxidation currents and basic pH of the solution will lead to an etching of the AlInN interlayer. From optical investigation, in figure 4.2 b), a sharp discontinuity between the central non oxidized part (purple in color) and the etched part (white external ring) can be observed. Moreover the observed roughness is due to the irregular etching. On the contrary, if low current regimes are adopted in combination with a basic pH solution, the process will lead to an oxidation of the AlInN. In this case the transition between the oxidized and non oxidized alloy will be more gradual as it can be seen in figure 4.3 c). Figures 4.3 d) and e) show a particular of the delimiting frame of the used mask. Together with the normal oxidation of the AlInN layer (figure 4.3 d), orange edge) damages to the sidewalls can occur due to the strain effects. Strain is generated in the heterostructure at the interface between the nitride alloys, typically due to lattice mismatch. In this case the SiO_2 capping layer is responsible for the strain. During the oxidation process, the interface between the capping layer and the (In, Al)GaN layers below it is more fragile and the built-in strain may lead to an undulation (figure 4.3 e)) or to the peeling (figure 4.3 f)) of the layers above the oxidized AlInN.

In any case, under proper conditions, the selective oxidation of LM AlInN can be achieved without any damage to the device structure

4.3 Current confinement in LED structures

Based on the oxidation process mentioned above InGaN/GaN LEDs with micron-scaled apertures (μLEDs), emitting at 440 nm, have been realized. The adopted electrical injection design resembles the one used in GaAs VCSEL structures. Annular *p*-type contact geometry is adopted in place of ITO contacts or semitransparent metallic spreading layers. The current confinement is achieved by inserting an AlInN interlayer used as carrier confinement layer after a lateral oxidation process [18].

Heterostructures were grown on 2 in. *c*-plane sapphire substrates. The sample consists of a 2 μm *n*-GaN layer ([Si]~3×10^{18} cm^{-3}, $\rho = 5\times10^{-3}$ Ω·cm), an $Al_{0.82}In_{0.18}N$ oxidation layer (25 nm thick, lattice matched (LM) to GaN and *n*-doped ([Si]~1×10^{19} cm^{-3}) to improve its electrical characteristics) used for the definition of current

apertures, a 10 nm GaN:Si spacer, a 3 period $In_{0.14}Ga_{0.86}N$ (3 nm)/GaN:Si (10 nm) multiple quantum well (MQW) active region, a 20 nm $Al_{0.2}Ga_{0.8}N$:Mg electron-barrier and a 170 nm *p*-GaN layer ([Mg]~2×10^{19} cm^{-3}, ρ= 0.34 Ω·cm). The layer thicknesses are chosen to match that of an ideal $5\lambda/2$ vertical cavity structure. The position of the oxidation layer on the *n*-type side is dictated by the current impossibility to grow *p*-doped AlInN layers. After thermal Mg activation, a SiO_2 mask is deposited on the wafer and circular mesas, 20 μm in diameter, are etched by Cl_2/Ar reactive ion etching down to a depth of 400 nm, giving access to the *n*-GaN bottom layer and the AlInN layer sidewall. Lateral anodic oxidation of AlInN is then performed in a NTA/KOH solution as explained before. The next processing steps are the deposition of a Ti/Al/Ni/Au *n*-contact and a Ni/Au *p*-contact, followed by the deposition of a SiO_2 passivation layer with contact openings and, finally, the realization of Ti/Au large contact pads.

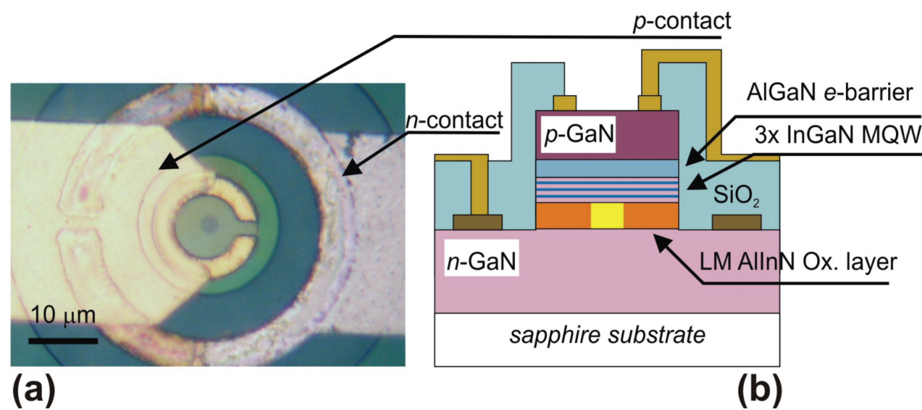


Figure 4.4: (a) Picture of the complete device and (b) schematic cross section of the device structure.

Figure 4.4 a) shows a top view of the device and figure 4.4 b) a schematic cross section of the structures fabricated for this work. The selective oxidation of AlInN allowed defining current apertures with diameters from 5 μm down to 1 μm. The device characterization was carried out mainly on structures with 3 μm current apertures.